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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,032	03/11/2002	Michael Nicolaidis	514842000100	9437

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	17

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/936,032	NICOLAIDIS, MICHAEL	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The foreign priority claim filed on 03/11/2002 was not entered because the foreign priority claim was not filed during the time period set forth in 37 CFR 1.55(a)(1). For original applications filed under 35 U.S.C. 111(a) (other than a design application) on or after November 29, 2000, the time period is during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. For applications that have entered national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and the Regulations under the PCT. See 37 CFR 1.55(a)(1)(ii). If applicant desires priority under 35 U.S.C. 119(a)-(d), (f) or 365(a) based upon a prior foreign application, applicant must file a petition for an unintentionally delayed priority claim (37 CFR 1.55(c)). The petition must be accompanied by (1) the claim (i.e., the claim required by 35 U.S.C. 119(a)-(d) and (f) and 37 CFR 1.55) for priority to the prior foreign application, unless previously submitted; (2) a surcharge under 37 CFR 1.17(t); and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.55(a)(1) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Specification

2. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart et al. (US 4,464,754).

Stewart et al. anticipate claim 1.

Stewart et al. teach a circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A), characterized in that it includes:

a circuit (20, 11) for generating an error control code for said output; and

a memory element (24, 24') arranged at said output, controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect (figure 1, 2A, 2B, col. 1, lines 43-68, col. 2, lines 1-42, lines 65-68, col. 3, lines 1-3, lines 11-22, col. 4, lines 43-46, Stewart et al.).

- Stewart et al. anticipate claim 2.

Stewart et al. teach the protected circuit, characterized in that the error control code generation circuit includes a circuit (20) for calculating a parity bit (P) for said output (A) and a circuit (22) for checking the parity of the output and of the parity bit (figure 2B, col. 4, lines 43-57, Stewart et al.).

5. Claims 6, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ratti (GB 2037034 A).

Ratti anticipates claim 6.

Ratti teaches a circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70,92) rated by a clock (CK), characterized in that it includes a second flip-flop (71, 93) connected to said output and rated by the clock delayed by a predetermined duration (8), and a circuit (74, 95) for analyzing the outputs of the flip-flops, and in that the analysis circuit (95) indicates an error if the flip-flop outputs are different (page 2, lines 28-48, Ratti).

- Ratti anticipates claim 8.

Ratti teaches a circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70) rated by a clock (CK),

characterized in that it includes a second flip-flop (71) rated by the clock and receiving said output delayed by a predetermined duration (8), and a circuit (74) for analyzing the flip-flop outputs, and in that the analysis circuit indicates an error if the flip-flop outputs are different (page 2, lines 28-48, Ratti).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart et al. (US 4,464,754) as applied to claim 1 above, and further in view of Paschal et al. (US 4,093,878).

As per claim 3, Stewart et al. substantially teach the claimed invention described in claim 1 (as rejected above). Stewart et al. teach the error control code generation circuit (figure 2B, col. 4, lines 43-46, Stewart et al.). Stewart et al. teach a duplicated logic circuit (11) and the memory element (24'), (figure 1, 2A, 2B, col. 1, lines 43-68, col. 2, lines 1-42, Stewart et al.).

However Stewart et al. do not explicitly teach that the memory element (24') being provided to be transparent when the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical, and to keep its state when the outputs are different.

Paschal et al. in an analogous art teach that in operation, the input logic gate changes state upon the coincidence of input signals, which change in state causes the integrator to change output level at a controlled rate (abstract, Paschal et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Stewart et al.'s patent with the teachings of Paschal et al. by including an additional step of using the memory element (24') being provided to be transparent when the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical, and to keep its state when the outputs are different. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the memory element (24') being provided to be transparent when the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical, and to keep its state when the outputs are different would provide the opportunity to remove the error condition in a signal at the output of a logic circuit and provide error-free signal.

- As per claim 4, Stewart et al. (US 4,464,754) and Paschal et al. (US 4,093,878) teach the additional limitations.

Stewart et al. teaches the error control code generation circuit (figure 2B, col. 4, lines 43-46, Stewart et al.). Paschal et al. teach an element (90) for delaying said output by a predetermined duration greater than the maximum duration of transient errors (col. 2, lines 1-4, Paschal et al.). Paschal et al. teach memory element (24') being provided to be transparent when the outputs of the logic circuit and of the delay element are identical, and to keep its state when said outputs are different (abstract, Paschal et al.).

- As per claim 5, Stewart et al. (US 4,464,754) and Paschal et al. (US 4,093,878) teach the additional limitations.

Stewart et al. teach that the memory element (24') is formed from a logic gate providing the output of the logic circuit, this logic gate including at least two first transistors (MN1, MP2) controlled by a signal (a) of the logic circuit and at least two second transistors (MP1, MN2) controlled by the corresponding signal (a*) of the duplicated circuit, each of the second transistors being connected in series with a respective one of the first transistors (figure 2B, col. 5, lines 16-21, lines 45-55, Stewart et al.).

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ratti (GB 2037034 A) as applied to claim 6 above, and further in view of Ewen et al. (US 5,301,196).

As per claim 7, Ratti substantially teach the claimed invention described in claim 6 (as rejected above).

However Ratti does not explicitly teach the specific use of the protected circuit, characterized in that the second flip-flop (93) is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

Ewen et al. in an analogous art teach that the outputs of these flip-flops, each triggered by a different edge of the clock, make up two demultiplexed data streams (abstract, Ewen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ratti's patent with the teachings of Ewen et al. by including an additional step of using the protected circuit, characterized in that the second flip-flop (93) is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to delay the output of the second flip-flop circuit and provide two signal outputs from the two flip-flops that can be compared.

10. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahey et al. (WO 97/40579) in view of Paschal et al. (US 4,093,878).

As per claim 9, Lahey et al. teach a circuit protected against transient disturbances, including three identical logic circuits (10a, 11a, 10b), characterized in that each of the logic circuits is preceded by a two-input memory element (24a, 24b, 24c) respectively receiving the outputs of the two other logic circuits (page 2, lines 7-16, Lahey et al.).

However Lahey et al. do not explicitly teach each memory element being provided to be transparent when its two inputs are identical, and to keep its state when the two inputs are different.

Paschal et al. in an analogous art teach that in operation, the input logic gate changes state upon the coincidence of input signals, which change in state causes the integrator to change output level at a controlled rate (abstract, Paschal et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahey et al.'s patent with the teachings of Paschal et al. by including an additional step of

using each memory element being provided to be transparent when its two inputs are identical, and to keep its state when the two inputs are different.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using each memory element being provided to be transparent when its two inputs are identical, and to keep its state when the two inputs are different would provide the opportunity to remove the error condition in a signal at the output of a logic circuit and provide error-free signal.

- As per claim 10, Lahey et al. and Paschal et al. teach the additional limitations.

Lahey et al. teach the protected circuit, characterized in that the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and the second input of the memory element being connected to the gates of the two other transistors (figure 3, page 6, lines 10-19, Lahey et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

Gary J. Lamarre
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